TEXAS INSTRUMENTS
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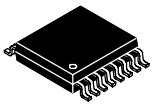


Actual Size
(5,1 mm x 4,9 mm)

TPS61130
TPS61131
TPS61132

SLVS431 – JUNE 2002

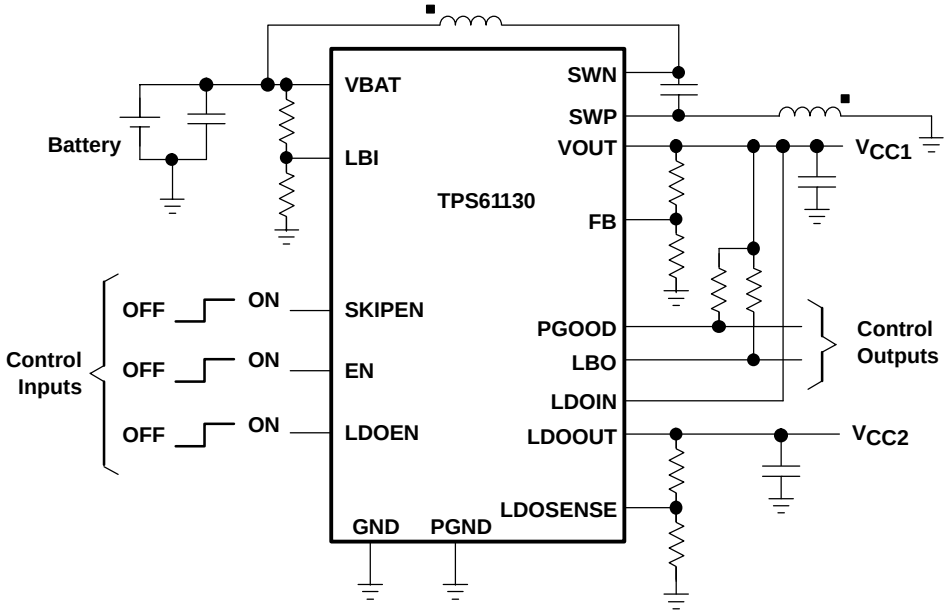
DUAL-OUTPUT, SINGLE-CELL LI OR DUAL CELL SEPIC CONVERTER

FEATURES

- **Synchronous, Up To 90% Efficient, SEPIC Converter With 300-mA Output Current From 2.5-V Input**
- **Integrated 200-mA LDO With Reverse Voltage Protected for DC/DC Output Voltage Post Regulation or Second Output Voltage**
- **Dual Input or Dual Output Mode**
- **TSSOP-16 Package**
- **40-μA (Typical) Total Device Quiescent Current**
- **1.8-V to 5.5-V Input Voltage Range**
- **Adjustable Output Voltage up to 5.5-V Fixed Output Voltage Options**
- **Power Save Mode for Improved Efficiency at Low Output Power**
- **Simple Li-Ion to 3.3-V Conversion**
- **Low Battery Comparator**
- **Power Good Output**
- **Low EMI-Converter (Integrated Antiringing Switch)**
- **Load Disconnect During Shutdown**
- **Overtemperature Protection**
- **EVM Available (TPS6113XEVM–206)**

APPLICATIONS

- **All Single Cell Li or Dual Cell Battery Operated Products as MP-3 Player, PDAs, and Other Portable Equipment**



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

DESCRIPTION

The TPS6113x devices provide a complete power supply solution for products powered by either a one-cell Li-Ion or Li-Polymer or a two-cell Alkaline, NiCd or NiMH batteries. The converter can generate two stable output voltages that are either adjusted by an external resistor divider or fixed internally on the chip. It also provides a simple solution for generating 3.3 V out of the one-cell Li-Ion or Li-Polymer battery at a maximum output current of at least 300 mA with supply voltages down to 1.8 V. The implemented SEPIC converter is based on a fixed frequency, pulse-width-modulation (PWM) controller using a synchronous rectifier to obtain maximum efficiency.

The maximum peak current in the SEPIC switch is limited to a value of 1600 mA.

The converter can be disabled to minimize battery drain. During shutdown, the load is completely disconnected from the battery. A low-EMI mode is implemented to reduce ringing and in effect lower radiated electromagnetic energy when the converter enters the discontinuous conduction mode. A power good output at the boost stage provides additional control of cascaded power supply components.

The built-in LDO can be used for a second output voltage derived either from the SEPIC output or directly from the battery. The output voltage of this LDO can be programmed by an external resistor divider or is fixed internally on the chip. The LDO can be enabled separately i.e., using the power good of the SEPIC stage.

The device is packaged in a 16-pin TSSOP (16 PW) package.

ORDERING INFORMATION

PACKAGE	CODE
16-Pin TSSOP	PW

AVAILABLE OUTPUT VOLTAGE OPTIONS(1)

T_A	OUTPUT VOLTAGE DC/DC	OUTPUT VOLTAGE LDO	PART NUMBER(2)
–40°C to 85°C	Adjustable	Adjustable	TPS61130PW
	3.3 V	3.3 V	TPS61131PW
	3.3 V	1.5 V	TPS61132PW

(1) Contact the factory to check availability of other fixed output voltage versions.
(2) The PW package is available taped and reeled. Add R suffix to device type (e.g., TPS61130PWR) to order quantities of 2000 devices per reel.

ABSOLUTE MAXIMUM RATINGS

over operating free-air temperature range unless otherwise noted(1)

	TPS61130 TPS61131 TPS61132
Input voltage range on FB	–0.3 V to 3.6 V
Input voltage range on SWN, VOUT, LDOIN, LDOOUT, LDOEN, LDOSENSE, PGOOD, LBO, VBAT, LBI, SKIPEN, EN	–0.3 V to 7 V
Continuous total power dissipation	See Dissipation Rating Table
Operating free air temperature range T_A	–25°C to 85°C
Maximum junction temperature T_J	150°C
Storage temperature range T_{stg}	–65°C to 150°C
Lead temperature 1,6 mm (1/16 inch) from case for 10s	260°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

	MIN	NOM	MAX	UNIT
Supply voltage at VBAT, V_I	1.8		5.5	V
Maximum LDO output current, I_O	200			mA
DC/DC—inductor, L	10	22		µH
DC/DC—input capacitor, C_i		10		µF
DC/DC—output capacitor, C_o	22	100		µF
LDO—input capacitor, C_i		1		µF
LDO—output capacitor, C_o	1	2.2		µF
Operating virtual junction temperature, T_J	–40		125	°C

ELECTRICAL CHARACTERISTICS

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

DC/DC STAGE							
PARAMETER			**TEST CONDITIONS**	**MIN**	**TYP**	**MAX**	**UNIT**
V_I	Input voltage range			1.8		5.5	V
V_O	Output voltage			2.5		5.5	V
V_{ref}	Reference voltage			485	500	515	mV
f	Oscillator frequency			400	500	600	kHz
	Switch current limit		VOUT= 3.3 V	1100	1300	1600	mA
	Startup current limit				520		mA
	SWN switch on resistance		VOUT= 3.3 V		200	350	mΩ
	SWP switch on resistance		VOUT= 3.3 V		250	500	mΩ
	Total accuracy					3	%
	DC/DC quiescent current	VBAT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 3.3 V, ENLDO = 0		10	25	µA
		VOUT	I_O = 0 mA, V_{EN} = VBAT = 1.8 V, VOUT = 3.3 V, ENLDO = 0		10	25	µA
	DC/DC shutdown current		V_{EN} = 0 V		0.2	1	µA

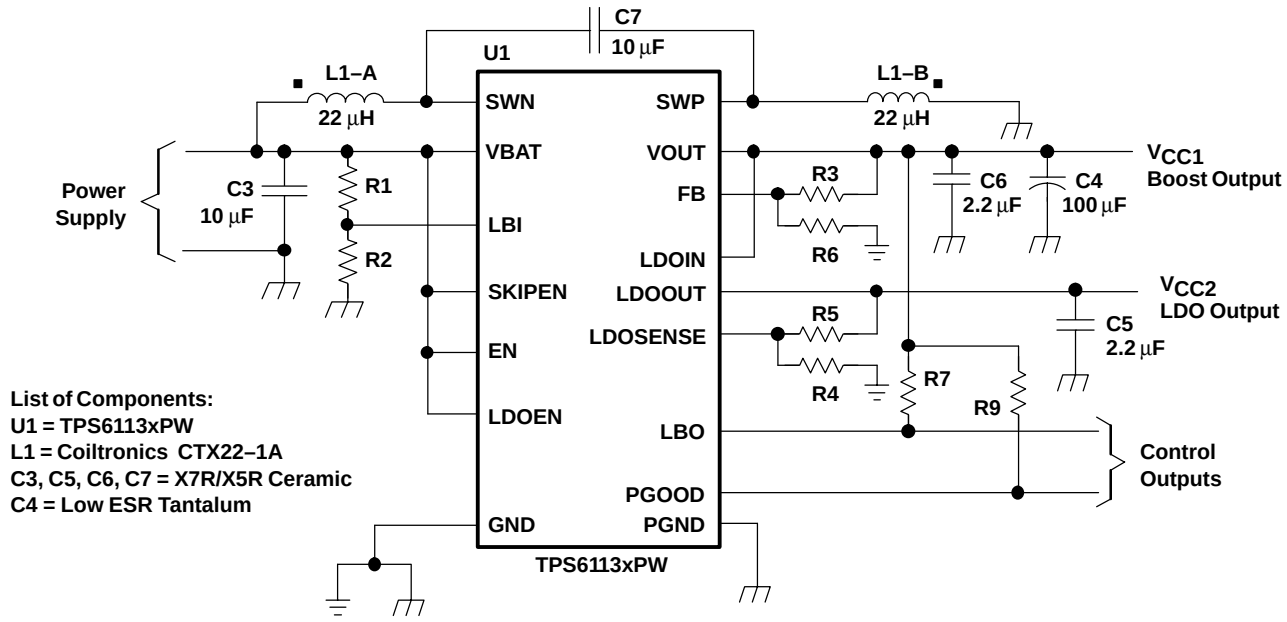
ELECTRICAL CHARACTERISTICS (continued)

over recommended free-air temperature range and over recommended input voltage range (typical at an ambient temperature range of 25°C) (unless otherwise noted)

LDO STAGE						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
$V_{I(LDO)}$	Input voltage range		1.8		7	V
$V_{O(LDO)}$	Output voltage		0.9		5.5	V
$I_{O(max)}$	Output current		200	320		mA
	LDO short circuit current limit				500	mA
	Minimum voltage drop	I_O = 200 mA			300	mV
	Total accuracy	$I_O \geq 1$ mA			±3%	
	Line regulation	LDOIN change from 1.8 V to 2.6 V at 100 mA, LDOOUT = 1.5 V			0.6%	
	Load regulation	Load change from 10% to 90%, LDOIN = 3.3 V			0.6%	
	LDO quiescent current	LDOIN = 7 V, VBAT = 1.8 V, EN = VBAT		20	30	µA
	LDO shutdown current	LDOEN = 0 V, LDOIN = 7 V		0.1	1	µA

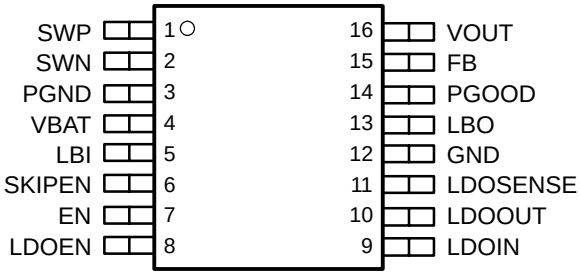
CONTROL STAGE						
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
V_{IL}	LBI voltage threshold	V_{LBI} voltage decreasing	490	500	510	mV
	LBI input hysteresis			10		mV
	LBI input current	EN = VBAT or GND		0.01	0.1	µA
	LBO output low voltage	V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	LBO output low current			100		µA
	LBO output leakage current	V_{LBO} = 7 V		0.01	0.1	µA
V_{IL}	EN, SKIPEN input low voltage				0.2 × VBAT	V
V_{IH}	EN, SKIPEN input high voltage		0.8 × VBAT			V
V_{IL}	LDOEN input low voltage				0.2 × V_{LDOIN}	V
V_{IH}	LDOEN input high voltage		0.8 × V_{LDOIN}			V
	EN, SKIPEN input current	Clamped on GND or VBAT		0.01	0.1	µA
	Powergood threshold	V_O = 3.3 V	0.9xV_O	0.92xV_O	0.95xV_O	V
	Powergood delay			30		µs
	Powergood output low voltage	V_O = 3.3 V, I_{OI} = 100 µA		0.04	0.4	V
	Powergood output low current			100		µA
	Powergood output leakage current	V_{PG} = 7 V		0.01	0.1	µA
	Overtemperature protection			140		°C
	Overtemperature hysteresis			20		°C

PARAMETER MEASUREMENT INFORMATION



PIN ASSIGNMENTS

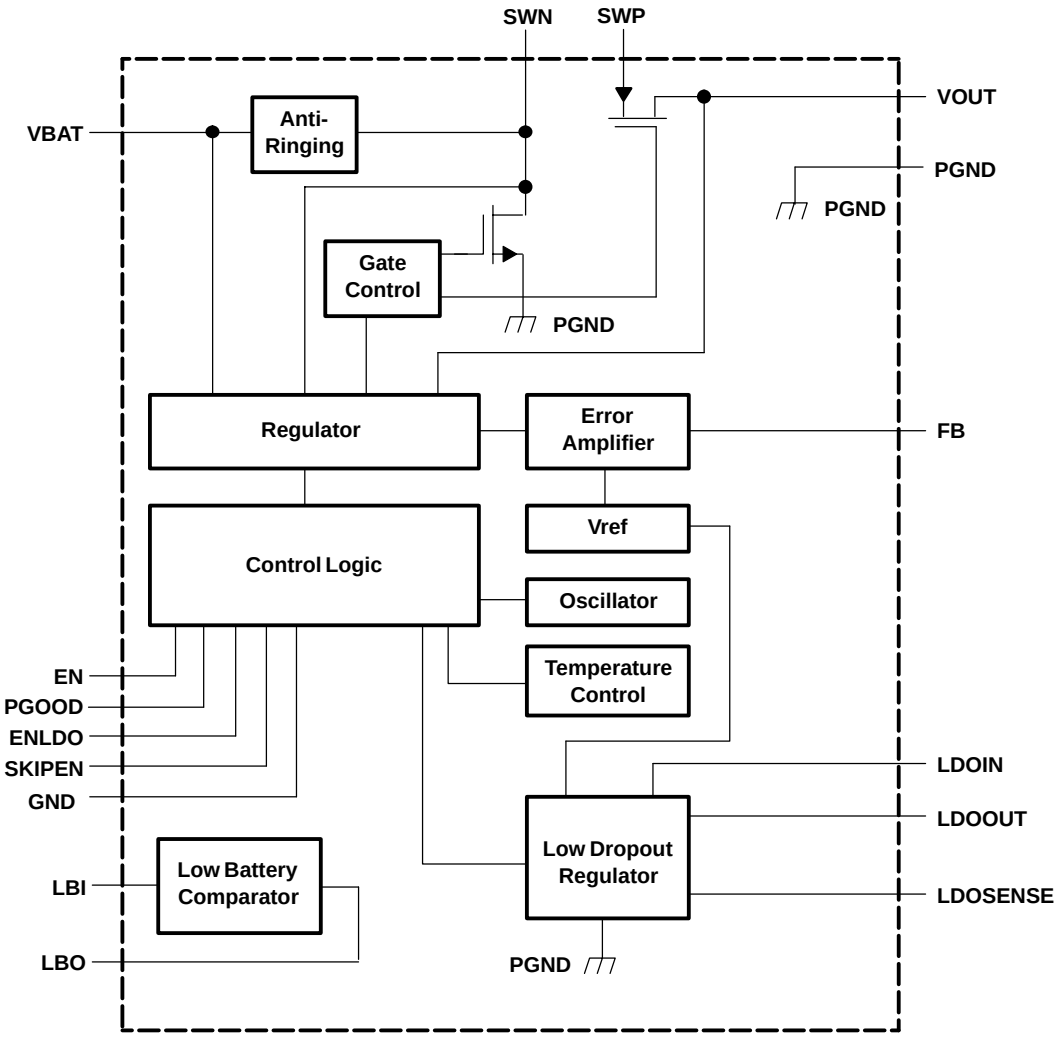
PW PACKAGE
(TOP VIEW)



Terminal Functions

TERMINAL		I/O	DESCRIPTION
NAME	NO.		
EN	7	I	DC/DC-enable input. (1/VBAT enabled, 0/GND disabled)
FB	15	I	DC/DC voltage feedback of adjustable versions
GND	12	I/O	Control/logic ground
LBI	5	I	Low battery comparator input (comparator enabled with EN)
LBO	13	O	Low battery comparator output (open drain)
LDOEN	8	I	LDO-enable input (1/LDOIN enabled, 0/GND disabled)
LDOOUT	10	O	LDO output
LDOIN	9	I	LDO input
LDOSENSE	11	I	LDO feedback for voltage adjustment, must be connected to LDOOUT at fixed output voltage versions
SWP	1	I	DC/DC rectifying switch input
PGND	3	I/O	Power ground
PGOOD	14	O	DC/DC output power good (1 : good, 0 : failure) (open drain)
SKIPEN	6	I	Enable/disable Power save mode (1: VBAT enabled, 0: GND disabled)
SWN	2	I	DC/DC switch input
VBAT	4	I	Supply pin
VOUT	16	O	DC/DC output

FUNCTIONAL BLOCK DIAGRAM



TYPICAL CHARACTERISTICS

TABLE OF GRAPHS

DC/DC CONVERTER		FIGURE
Maximum output current	vs Input voltage	1, 2
Efficiency	vs Output current (TPS61130) (V_O = 2.5 V, V_I = 1.8 V)	3
	vs Output current (TPS61132) (V_O = 3.3 V, V_I = 1.8 V, 3.8 V)	4
	vs Output current (TPS61130) (V_O = 5.0 V, V_I = 2.4 V, 3.3 V)	5
	vs Input voltage (TPS61132)	6
Output voltage	vs Output current (TPS61132)	7
No-load supply current into VBAT	vs Input voltage (TPS61132)	8
No-load supply current into VOUT	vs Input voltage (TPS61132)	9
Waveforms	Output voltage in continuous mode (TPS61132)	10
	Output voltage in power save mode (TPS61132)	11
	Load transient response (TPS61132)	12
	Line transient response (TPS61132)	13
	DC/DC converter start-up after enable (TPS61132)	14
LDO		
Maximum LDO output current	vs LDO input voltage (V_O = 2.5 V, 3.3 V)	15
	vs LDO input voltage (V_O = 1.5 V, 1.8 V)	16
LDO output voltage	vs LDO output current (TPS61131)	17
LDO dropout voltage	vs LDO output current (TPS61131, TPS61132)	18
Supply current into LDOIN	vs LDOIN input voltage (TPS61132)	19
PSRR	vs Frequency (TPS61132)	20
Waveforms	LDO load transient response	21
	LDO line transient response	22
	LDO start-up after enable	23

TYPICAL CHARACTERISTICS

MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

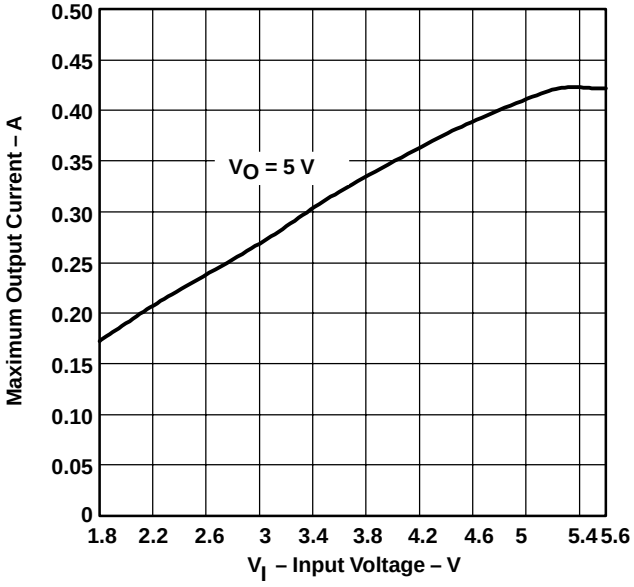


Figure 1

MAXIMUM OUTPUT CURRENT
vs
INPUT VOLTAGE

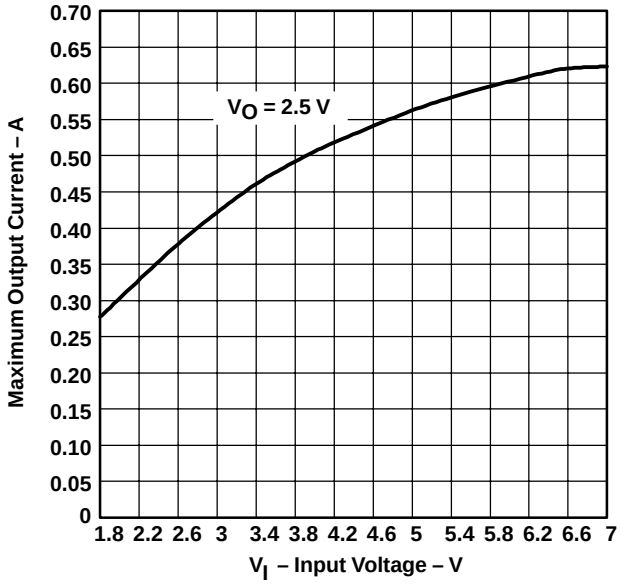


Figure 2

TPS61130
EFFICIENCY
vs
OUTPUT CURRENT

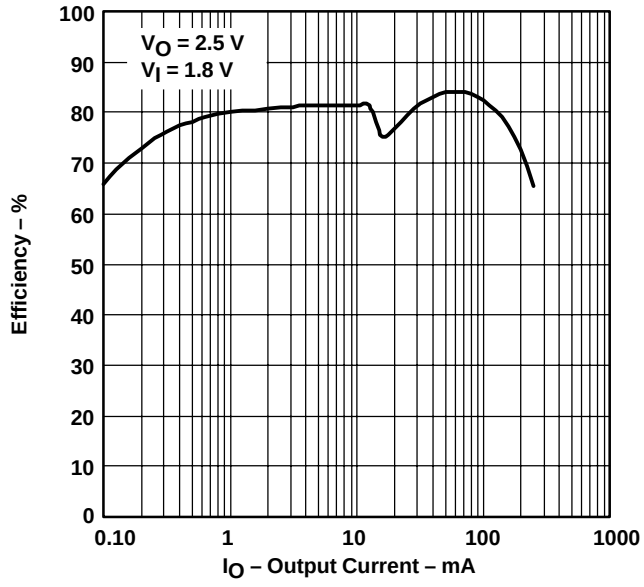


Figure 3

TPS61132
EFFICIENCY
vs
OUTPUT CURRENT

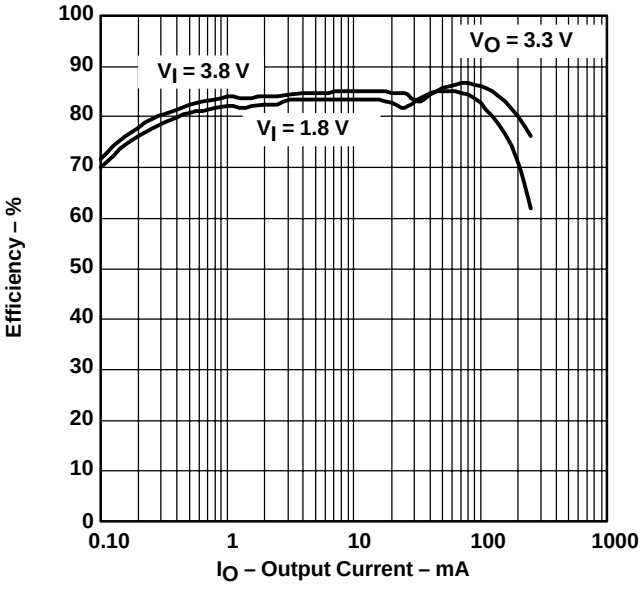


Figure 4

TYPICAL CHARACTERISTICS

TPS61130
EFFICIENCY
vs
OUTPUT CURRENT

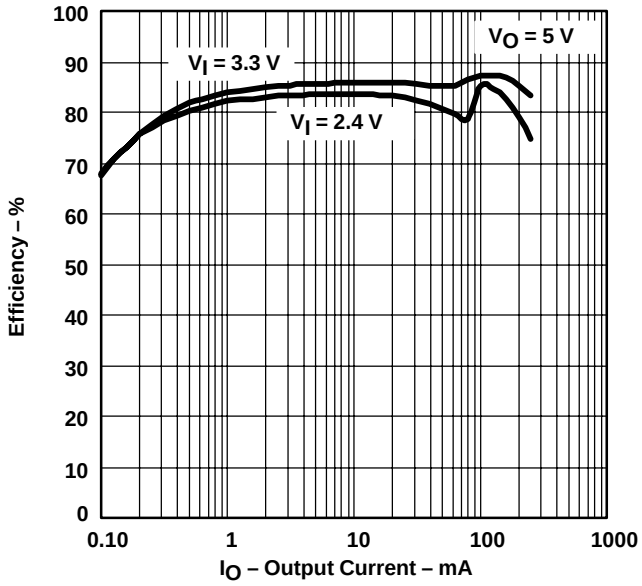


Figure 5

TPS61132
EFFICIENCY
vs
INPUT VOLTAGE

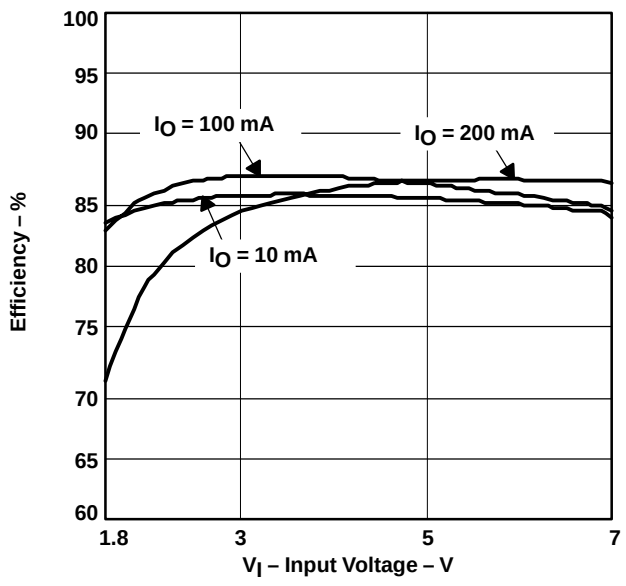


Figure 6

TPS61132
OUTPUT VOLTAGE
vs
OUTPUT CURRENT

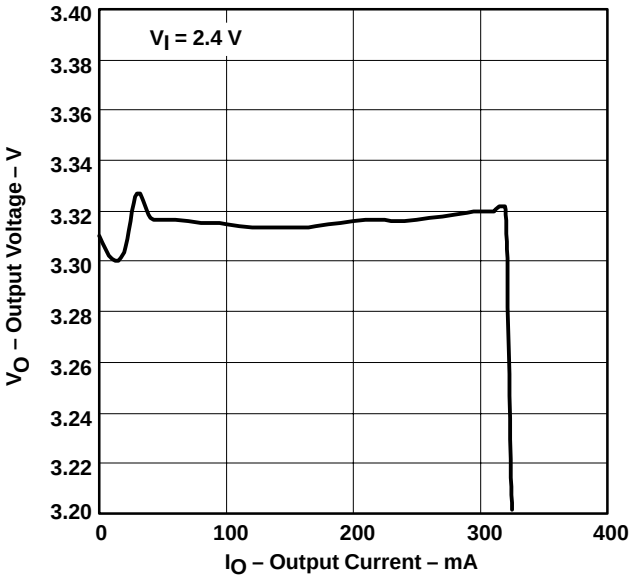


Figure 7

TPS61132
NO-LOAD SUPPLY CURRENT INTO VBAT
vs
INPUT VOLTAGE

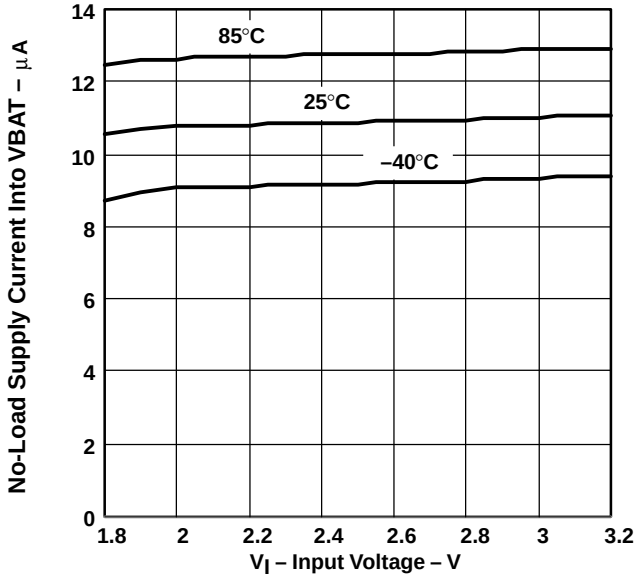


Figure 8

TYPICAL CHARACTERISTICS

TPS61132
NO-LOAD SUPPLY CURRENT INTO VOUT
VS
INPUT VOLTAGE

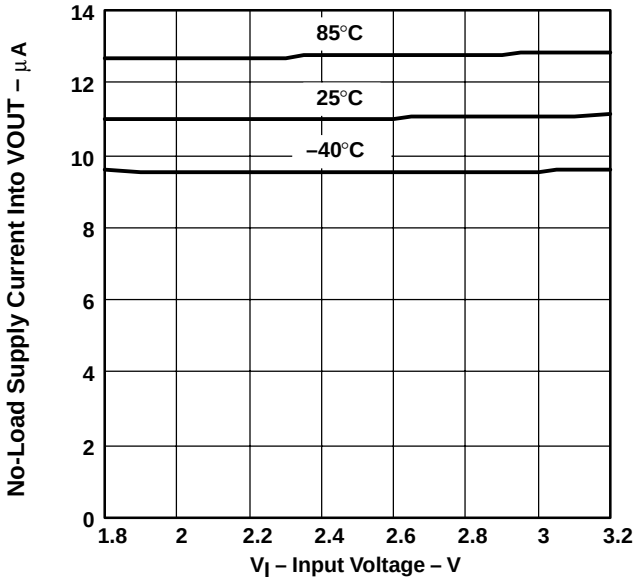


Figure 9

TPS61132
OUTPUT VOLTAGE IN CONTINUOUS MODE

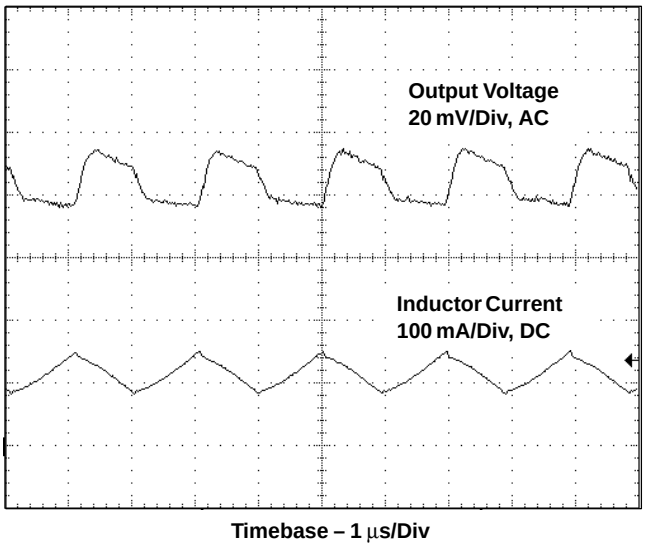


Figure 10

TPS61132
OUTPUT VOLTAGE IN POWER SAVE MODE

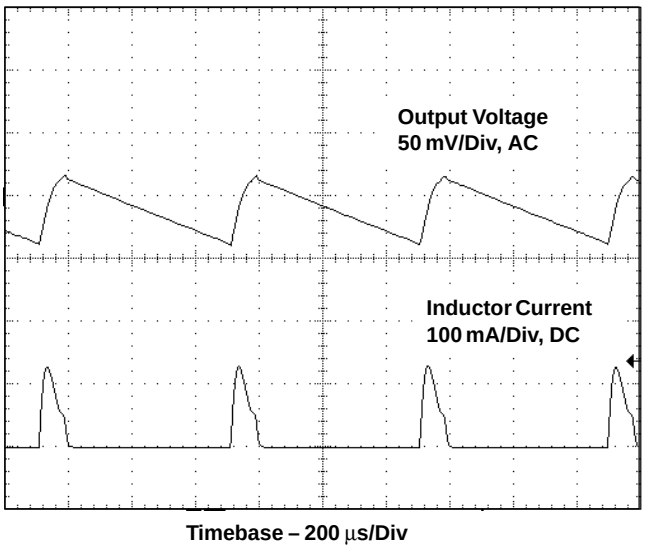


Figure 11

TPS61132
LOAD TRANSIENT RESPONSE

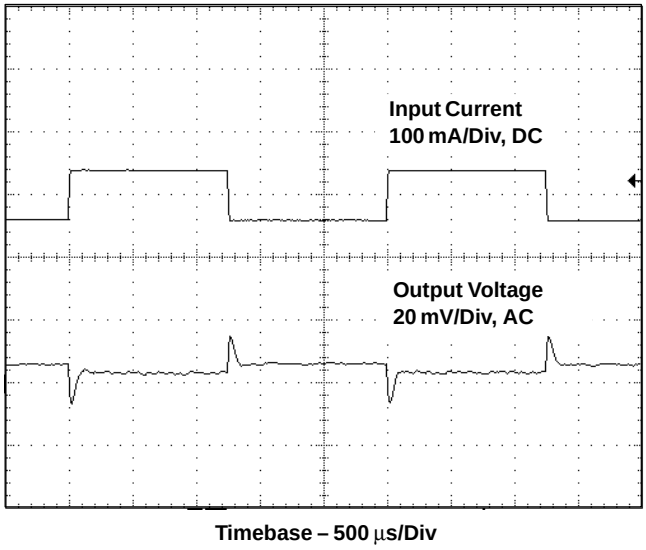


Figure 12

TYPICAL CHARACTERISTICS

TPS61132
LINE TRANSIENT RESPONSE

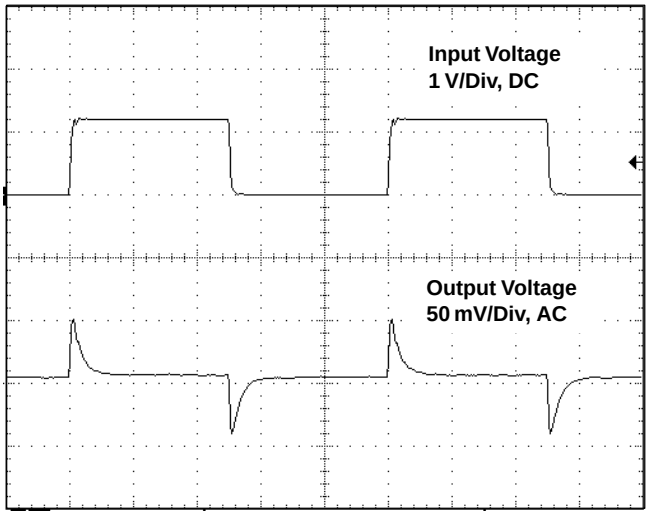


Figure 13

TPS61132
DC/DC CONVERTER START-UP AFTER ENABLE

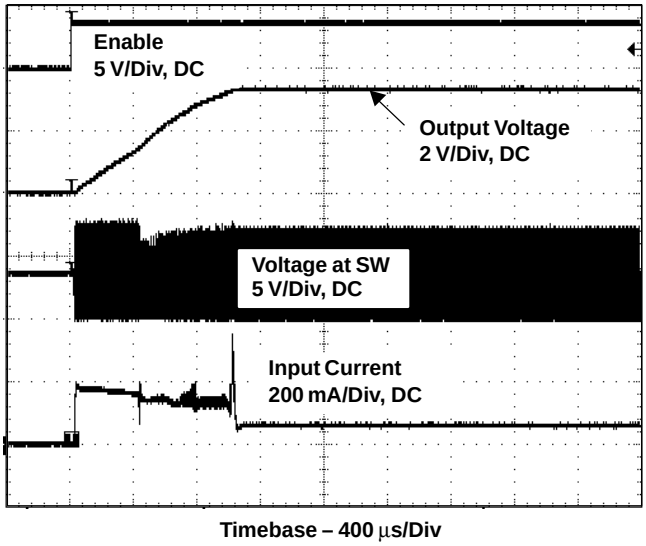


Figure 14

MAXIMUM LDO OUTPUT CURRENT
vs
LDO INPUT VOLTAGE

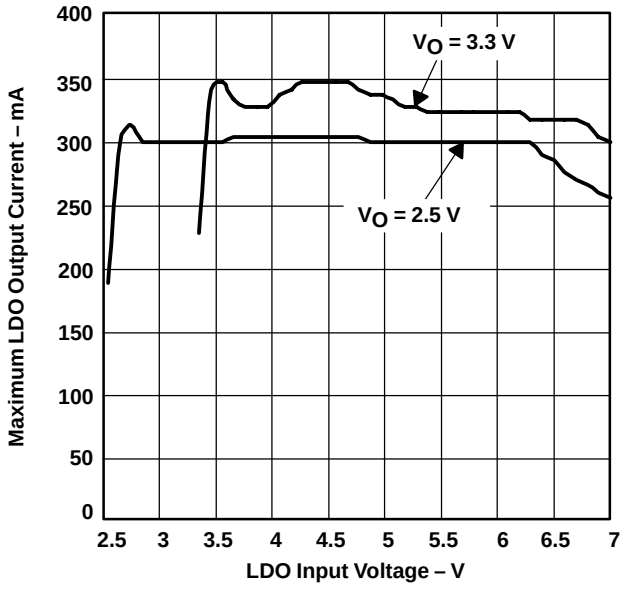


Figure 15

MAXIMUM LDO OUTPUT CURRENT
vs
LDO INPUT VOLTAGE

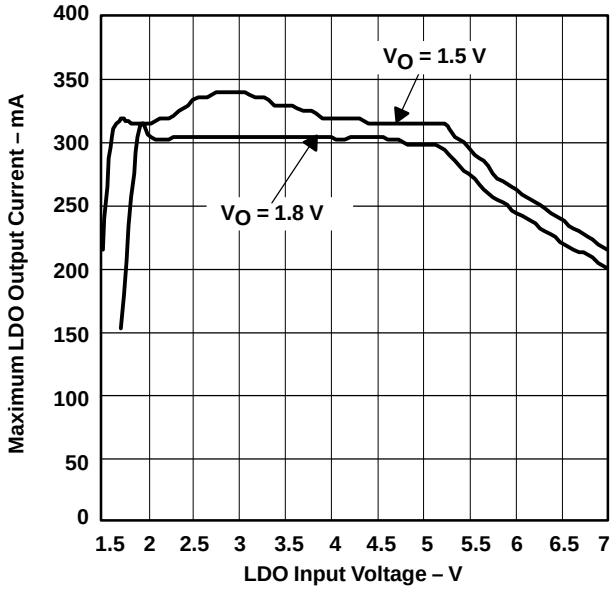


Figure 16

TYPICAL CHARACTERISTICS

TPS61131
LDO OUTPUT VOLTAGE
vs
LDO OUTPUT CURRENT

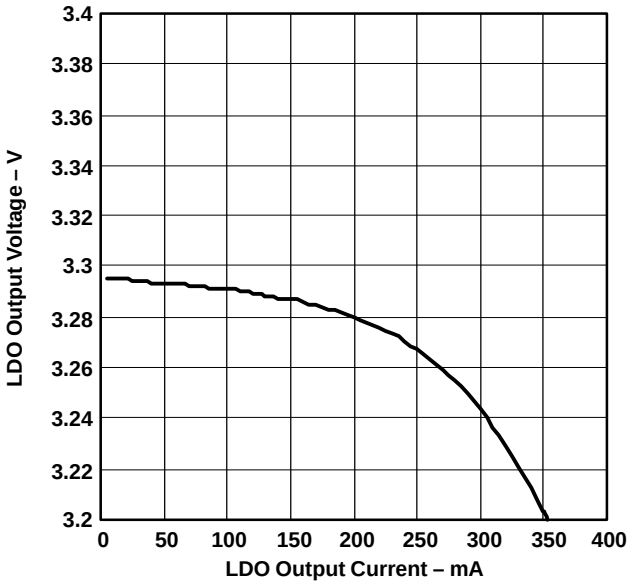


Figure 17

LDO DROPOUT VOLTAGE
vs
LDO OUTPUT CURRENT

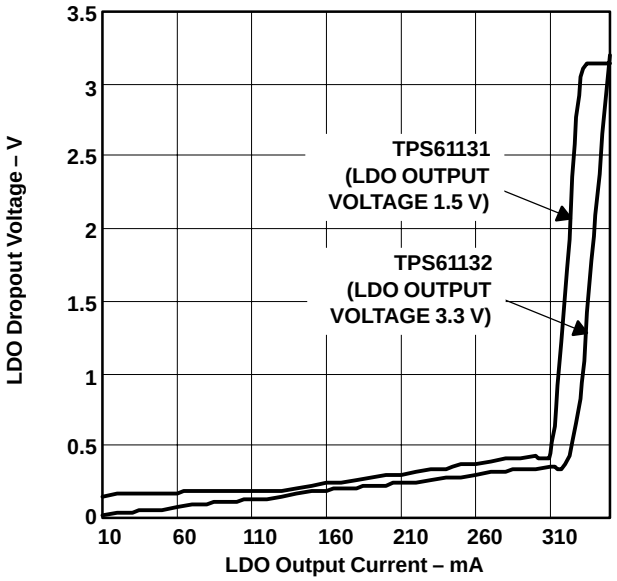


Figure 18

TPS61132
SUPPLY CURRENT INTO LDOIN
vs
LDOIN INPUT VOLTAGE

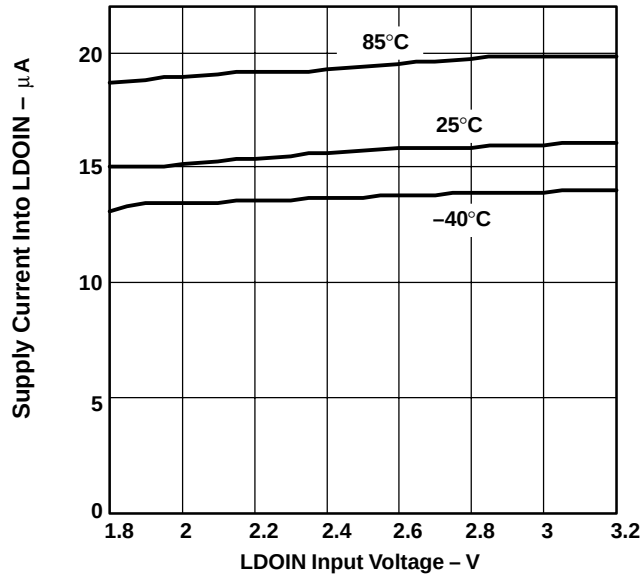


Figure 19

TPS61132
PSRR
vs
FREQUENCY

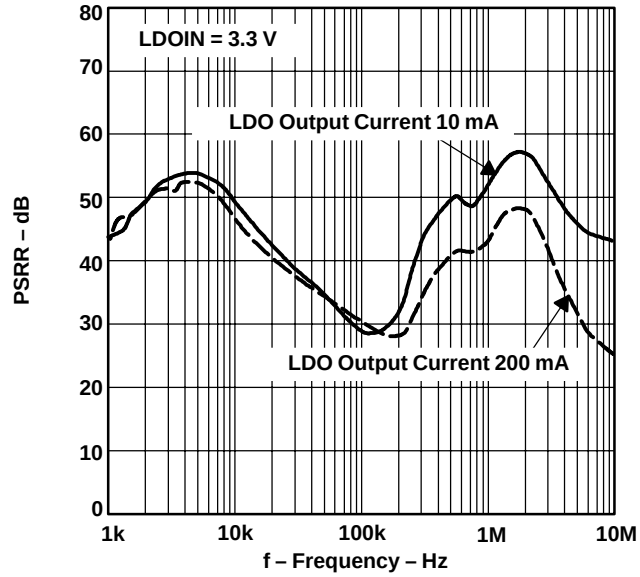
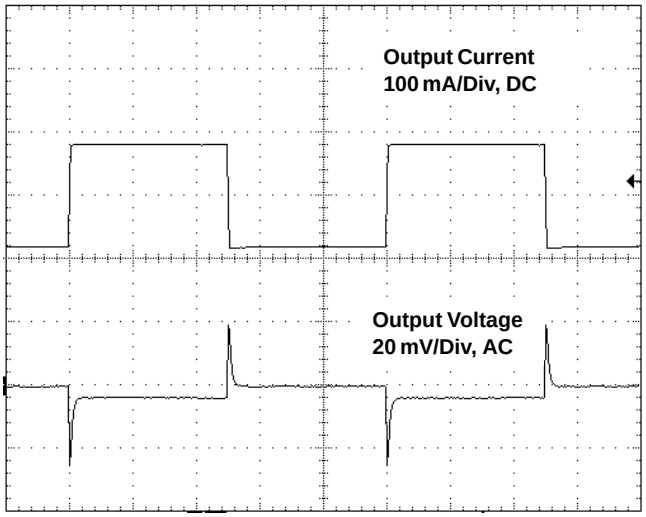


Figure 20

TYPICAL CHARACTERISTICS

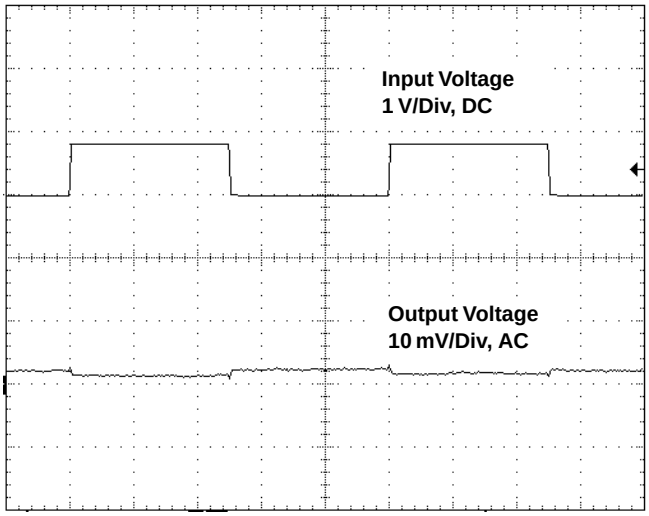
LDO LOAD TRANSIENT RESPONSE



Timebase – 500 μs/Div

Figure 21

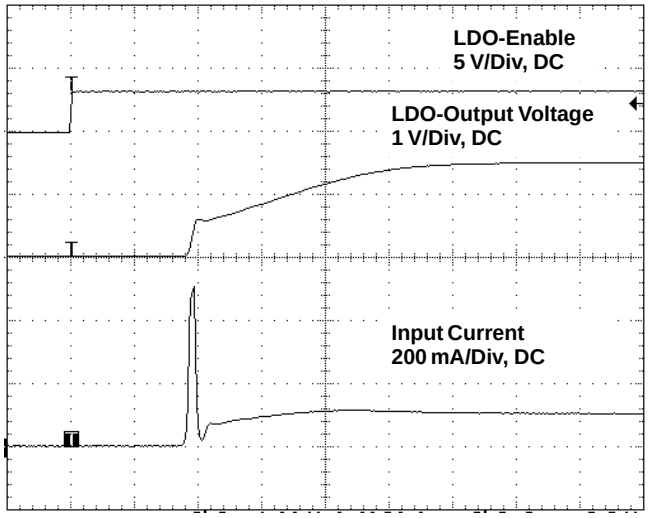
LDO LINE TRANSIENT RESPONSE



Timebase – 2 ms/Div

Figure 22

LDO START-UP AFTER ENABLE



Timebase – 20 μs/Div

Figure 23

APPLICATION INFORMATION

DESIGN PROCEDURE

The TPS6113x dc/dc converters are intended for systems powered by a dual-cell NiCd or NiMH battery with a typical terminal voltage between 1.8 V and 5.5 V. They can also be used in systems powered by one-cell Li–Ion with a typical stack voltage between 2.5 V and 4.2 V. Additionally, two or three primary and secondary alkaline battery cells can be the power source in systems where the TPS6113x is used.

Programming the Output Voltage

DC/DC Converter

The output voltage of the TPS61130 dc/dc converter section can be adjusted with an external resistor divider. The typical value of the voltage on the FB pin is 500 mV. The maximum allowed value for the output voltage is 5.5 V. The current through the resistive divider should be about 100 times greater than the current into the FB pin. The typical current into the FB pin is 0.01 μA and the voltage across R6 is typically 500 mV. Based on those two values, the recommended value for R6 should be lower than 500 kΩ, in order to set the divider current at 1 μA or higher. Because of internal compensation circuitry the value for this resistor should be in the range of 200 kΩ. From that, the value of resistor R3, depending on the needed output voltage (V_O), can be calculated using equation 1:

$$R3 = R6 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \quad (1)$$

If as an example, an output voltage of 3.3 V is needed, a 1-MΩ resistor should be chosen for R3.

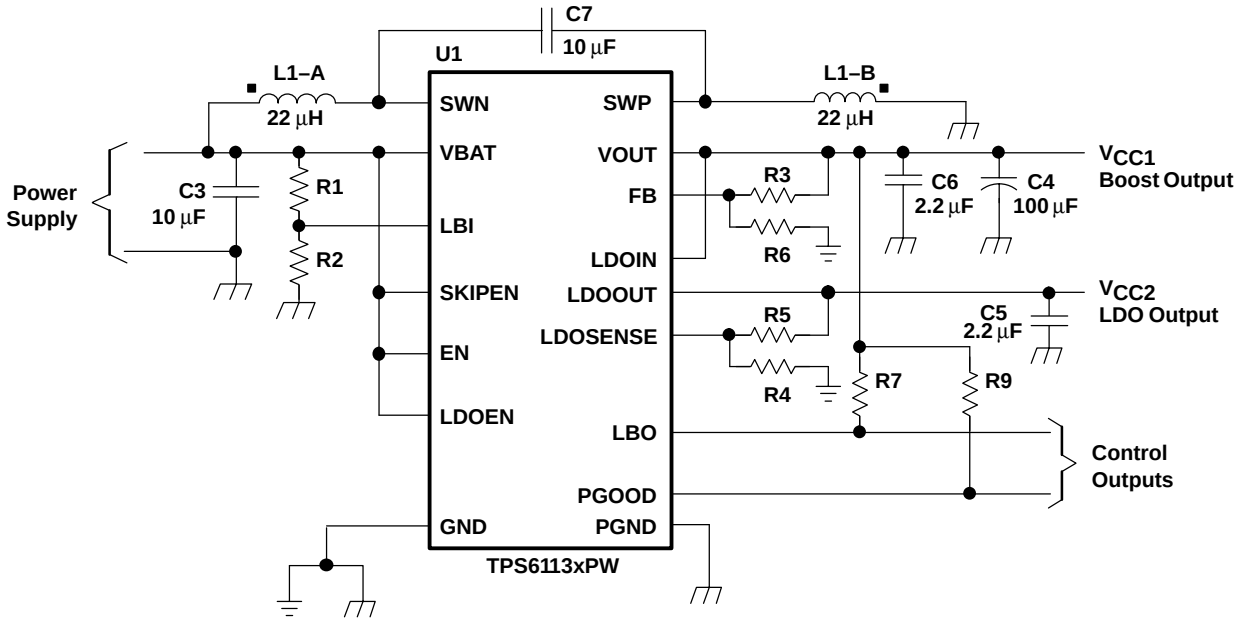


Figure 24. Typical Application Circuit for Adjustable Output Voltage Option

LDO

Programming the output voltage at the LDO follows almost the same rules as at the dc/dc converter section. The maximum programmable output voltage at the LDO is 5.5 V. Since reference and internal feedback circuitry are similar, as they are at the boost converter section, R4 also should be in the 200-kΩ range. The calculation of the value of R5 can be done using the following equation (2):

$$R5 = R4 \times \left(\frac{V_O}{V_{FB}} - 1\right) = 180\ k\Omega \times \left(\frac{V_O}{500\ mV} - 1\right) \quad (2)$$

If as an example, an output voltage of 1.5 V is needed, a 360 kΩ-resistor should be chosen for R5.

Programming the LBI/LBO Threshold Voltage

The current through the resistive divider should be about 100 times greater than the current into the LBI pin. The typical current into the LBI pin is 0.01 μA, and the voltage across R2 is equal to the LBI voltage threshold that is generated on-chip, which has a value of 500 mV. The recommended value for R2 is therefore in the range of 500 kΩ. From that, the value of resistor R1, depending on the desired minimum battery voltage $V_{BAT,}$ can be calculated using equation 3.

$$R1 = R2 \times \left(\frac{V_{BAT}}{V_{LBI-threshold}} - 1 \right) = 390\ k\Omega \times \left(\frac{V_{BAT}}{500\ mV} - 1 \right) \quad (3)$$

The output of the low battery supervisor is a simple open-drain output that goes active low if the dedicated battery voltage drops below the programmed threshold voltage on LBI. The output requires a pullup resistor with a recommended value of 1 MΩ. The maximum voltage which is used to pull up the LBO outputs should not exceed the output voltage of the dc/dc converter. If not used, the LBO pin can be left floating or tied to GND.

Inductor Selection

A SEPIC converter normally requires three main passive components for storing energy during the conversion. Two inductors, a flying capacitor, and a storage capacitor at the output are required. To select the two inductor, it is recommended to keep the possible peak inductor current below the current limit threshold of the power switch in the chosen configuration. For example, the current limit threshold of the TPS6113x's switch is 1200 mA at an output voltage of 3.3 V. The highest peak current through the switch is the sum of the two inductors current and depends on the output load, the input (V_{BAT}), and the output voltage (V_{OUT}). Estimation of the maximum average inductor current can be done using equation 4:

$$I_{L1-A} = I_{L1-B} = I_{OUT} \times \frac{V_{OUT}}{V_{BAT} \times 0.8} \quad (4)$$

For example, for an output current of 100 mA at 3.3 V, at least 230 mA of current flows through the inductor at a minimum input voltage of 1.8 V.

The second parameter for choosing the inductor is the desired current ripple in the inductor. Normally, it is advisable to work with a ripple of less than ±20% of the average inductor current. A smaller ripple reduces the magnetic hysteresis losses in the inductor, as well as output voltage ripple and EMI. But in the same way, regulation time at load changes rises. In addition, a larger inductor increases the total system costs. With those parameters, it is possible to calculate the value for the inductor by using equation 5:

$$L1 - A = L1 - B = \frac{V_{BAT} \times V_{OUT}}{\Delta I_L \times f \times \left(V_{OUT} + V_{BAT} \right)} \quad (5)$$

Parameter f is the switching frequency and ΔI_L is the ripple current in the inductor, i.e., $0.4 \times I_L$. In this example, the desired inductor has the value of 25 μH. With this calculated value and the calculated currents, it is possible to choose a suitable inductor. Care has to be taken that load transients and losses in the circuit can lead to higher currents as estimated in equation 5. Also, the losses in the inductor caused by magnetic hysteresis losses and copper losses are a major parameter for total circuit efficiency.

The following inductor series from different suppliers were tested. All work with the TPS6113x converter within their specified parameters.

Table 1. Recommended Inductors

VENDOR	RECOMMENDED INDUCTOR SERIES	COUPLED INDUCTOR SERIES
Sumida	CDRH73	
	CDRH74	
	CDRH5D18	
	CDRH6D38	
Wurth Electronik	WE–PD type S	WE–DD
	WE–PD type M	
Coiltronics	DR73	CTX series
	DR74	
Murata	LQS66C	
	LQN6C	
TDK	SLF 7045	
	SLF 7032	

Capacitor Selection

Input Capacitor

At least a 10-µF input capacitor is recommended to improve transient behavior of the regulator and EMI behavior of the total power supply circuit. A ceramic capacitor or a tantalum capacitor with a 100-nF ceramic capacitor in parallel, placed close to the IC, is recommended.

Flying Capacitor DC/DC Converter

In the normal operating mode, the *flying* capacitor (C7) must be large enough so that the voltage across the capacitor is small. This means the resonance frequency formed by the *flying* capacitor and the inductors must be at least ten times lower than the switching frequency.

$$C_{min} = \frac{100}{4\pi^2 f^2 L} \quad (6)$$

Where L is the inductance of L1–A or L1–B.

To optimize efficiency, capacitors with very low ESR such as ceramic capacitors are recommended. The voltage rating of the *flying* capacitor must be higher than the input voltage V_{BAT}.

Output Capacitor DC/DC Converter

The major parameter necessary to define the output capacitor is the maximum allowed output voltage ripple of the converter. This ripple is determined by two parameters of the capacitor, the capacitance and the ESR. It is possible to calculate the minimum capacitance needed for the defined ripple, supposing that the ESR is zero, by using equation 7:

$$C_{min} = \frac{I_{OUT} \times V_{OUT}}{f \times \Delta V \times \left(V_{OUT} + V_{BAT}\right)} \quad (7)$$

Parameter *f* is the switching frequency and ΔV is the maximum allowed ripple.

With a chosen ripple voltage of 15 mV, a minimum capacitance of 22 µF is needed. The total ripple is larger due to the ESR of the output capacitor. This additional component of the ripple can be calculated using equation 8:

$$\Delta V_{ESR} = I_{OUT} \times R_{ESR} \quad (8)$$

An additional ripple of 10 mV is the result of using a tantalum capacitor with a low ESR of 100 mΩ. The total ripple is the sum of the ripple caused by the capacitance and the ripple caused by the ESR of the capacitor. In this example, the total ripple is 25 mV. It is possible to improve the design by enlarging the capacitor or using smaller capacitors in parallel to reduce the ESR or by using better capacitors with lower ESR, like ceramics. So, tradeoffs have to be made between performance and costs of the converter circuit.

Output Capacitor LDO

To ensure stable output regulation, it is required to use an output capacitor at the LDO output. We recommend using ceramic capacitors in the range from 1 µF up to 4.7 µF. At 4.7 µF and above it is recommended to use standard ESR tantalum. There is no maximum capacitance value.

Layout Considerations

For all switching power supplies, the layout is an important step in the design, especially at high peak currents and high switching frequencies. If the layout is not carefully done, the regulator could show stability problems as well as EMI problems. Therefore, use wide and short traces for the main current path and for the power ground tracks. The input capacitor, output capacitor, and the inductor should be placed as close as possible to the IC. Use a common ground node for power ground and a different one for control ground to minimize the effects of ground noise. Connect these ground nodes at any place close to one of the ground pins of the IC.

The feedback divider should be placed as close as possible to the control ground pin of the IC. To lay out the control ground, it is recommended to use short traces as well, separated from the power ground traces. This avoids ground shift problems, which can occur due to superimposition of power ground current and control ground current.

APPLICATION EXAMPLES

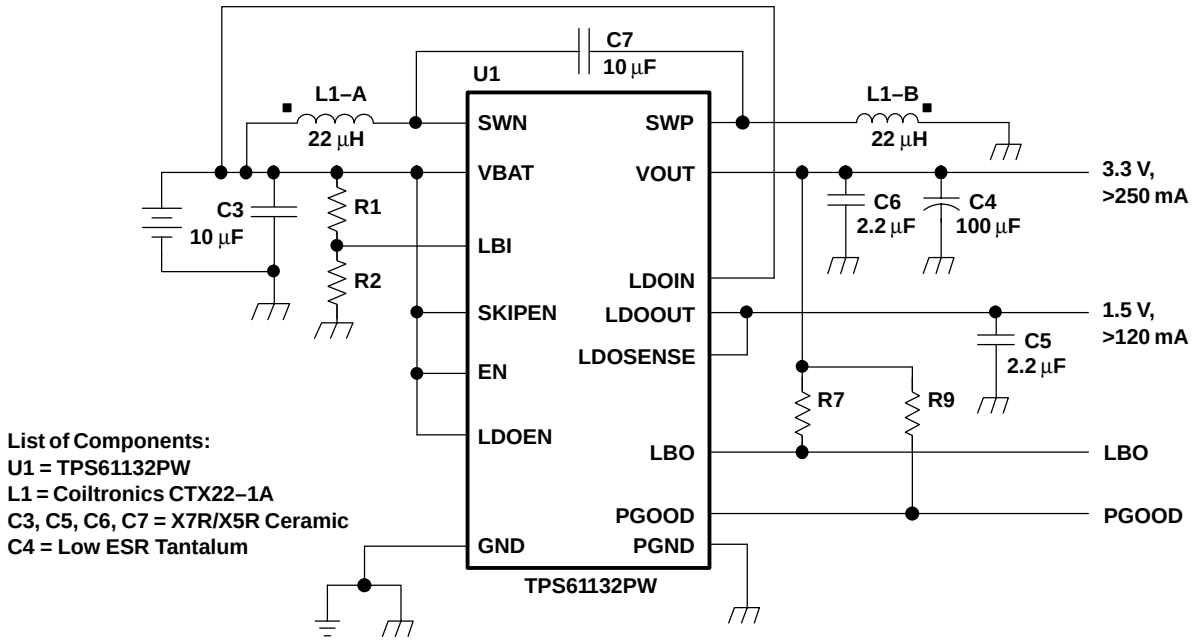
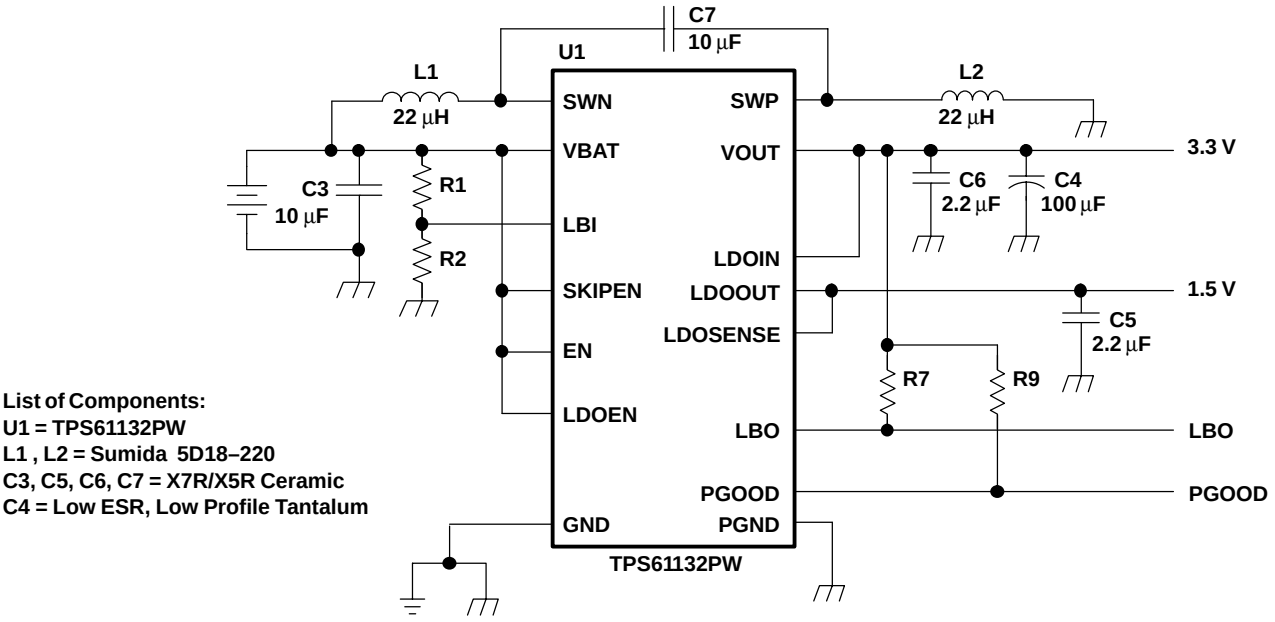


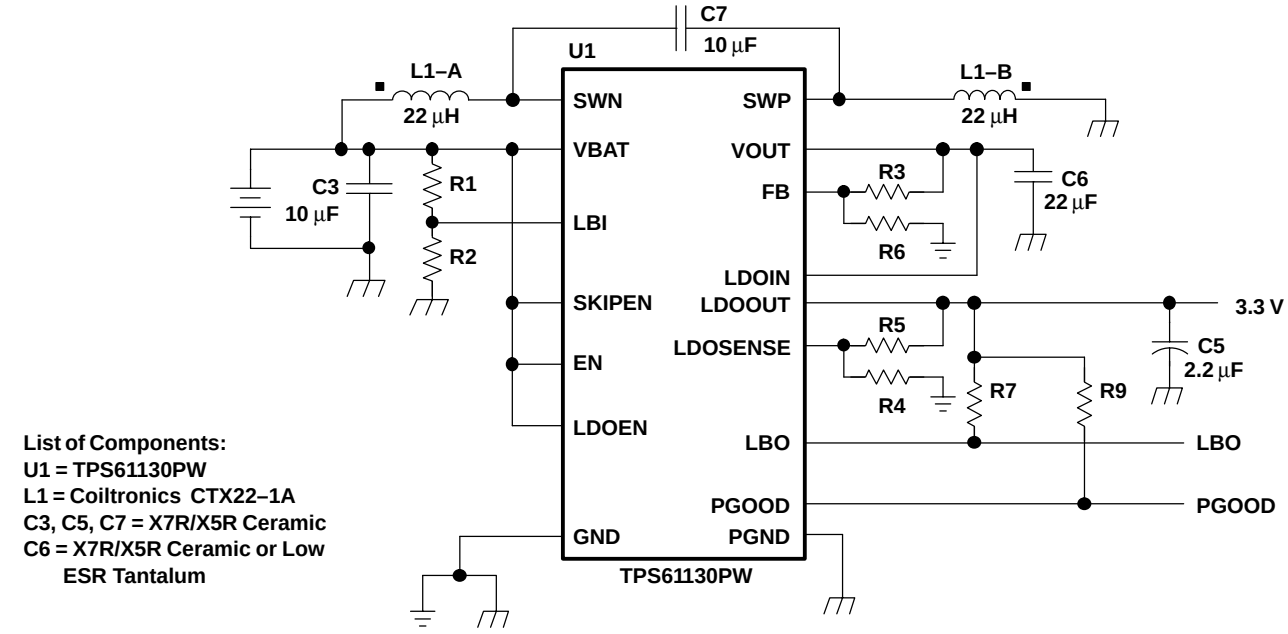
Figure 25. Solution for Maximum Output Power

APPLICATION INFORMATION



List of Components:
U1 = TPS61132PW
L1 , L2 = Sumida 5D18–220
C3, C5, C6, C7 = X7R/X5R Ceramic
C4 = Low ESR, Low Profile Tantalum

Figure 26. Low Profile Solution, Maximum Height 1,8 mm



List of Components:
U1 = TPS61130PW
L1 = Coiltronics CTX22–1A
C3, C5, C7 = X7R/X5R Ceramic
C6 = X7R/X5R Ceramic or Low ESR Tantalum

Figure 27. Single Output Using LDO as Filter

APPLICATION INFORMATION

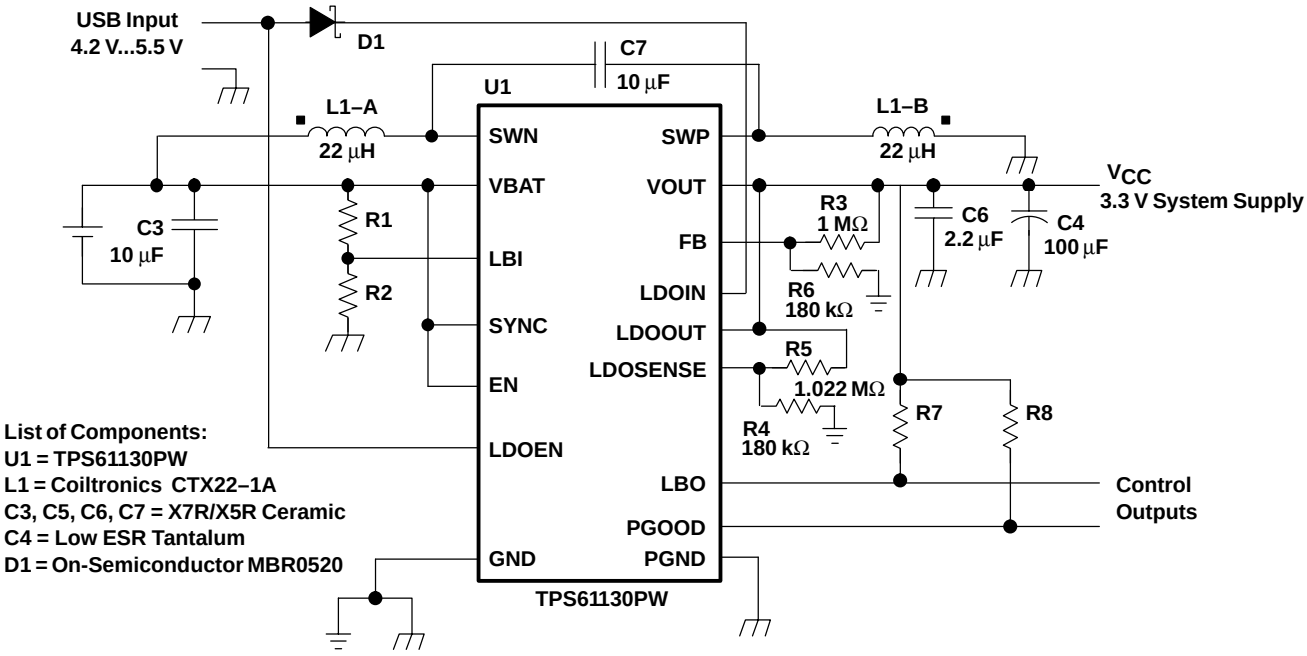


Figure 28. Dual Input Power Supply Solution

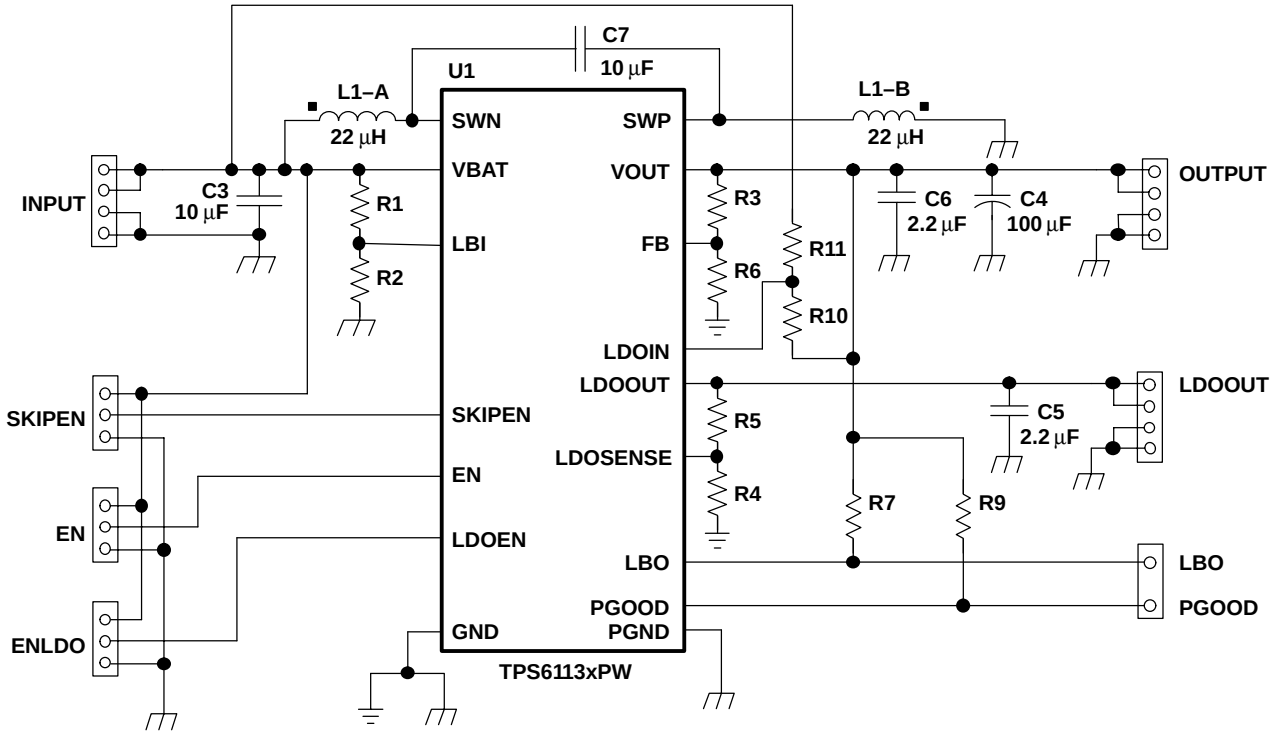


Figure 29. TPS6113x EVM Circuit Diagram

DETAILED DESCRIPTION

Synchronous Rectifier

The device integrates an N-channel and a P-channel MOSFET transistor to realize a synchronous rectifier. Because the commonly used discrete Schottky rectifier is replaced with a low RDS(ON) PMOS switch, the power conversion efficiency reaches 90%. To avoid ground shift due to the high currents in the NMOS switch, two separate ground pins are used. The reference for all control functions is the GND pin. The source of the NMOS switch is connected to PGND. Both grounds must be connected on the PCB at only one point close to the GND pin. Due to the nature of the SEPIC topology, there is no dc path from the battery to the output. No additional components must be added to the design to make sure the battery is disconnected from the output of the converter.

During shutdown (EN = low) the PMOS and its backgate diode are completely turned off by a special circuit.

Controller Circuit

The controller circuit of the device is based on a fixed frequency multiple feedforward controller topology. Input voltage, output voltage, and voltage drop on the NMOS switch are monitored and forwarded to the regulator. So changes in the operating conditions of the converter directly affect the duty cycle and must not take the indirect and slow way through the control loop and the error amplifier. The control loop, determined by the error amplifier, only has to handle small signal errors. The input for it is the feedback voltage on the FB pin or, at fixed output voltage versions, the voltage on the internal resistor divider. It is compared with the internal reference voltage to generate an accurate and stable output voltage.

The peak current of the NMOS switch is also sensed to limit the maximum current flowing through the switch and the inductor. The typical peak current limit is set to 1300 mA.

An internal temperature sensor prevents the device from getting overheated in case of excessive power dissipation.

Device Enable

The device is put into operation when EN is set high. It is put into a shutdown mode when EN is set to GND.

In shutdown mode, the regulator stops switching, all internal control circuitry including the low-battery comparator is switched off, and the load is isolated from the input (as described in the Synchronous Rectifier Section). This also means that the output voltage can drop below the input voltage during shutdown. During start-up of the converter, the duty cycle and the peak current are limited in order to avoid high peak currents drawn from the battery.

An undervoltage lockout function prevents device start-up if the supply voltage on VBAT is lower than approximately 1.6 V. When in operation and the battery is being discharged, the device automatically enters the shutdown mode if the voltage on VBAT drops below approximately 1.6 V. This undervoltage lockout function is implemented in order to prevent the malfunctioning of the converter.

LDO Enable

The LDO can be separately enabled and disabled by using the LDOEN pin in the same way as the EN pin at the dc/dc converter stage described above.

Power Good

The PGOOD pin stays high impedance when the dc/dc converter delivers an output voltage within a defined voltage window. So it can be used to enable any connected circuitry such as cascaded converters (LDO) or microprocessor circuits.

Skip Mode

The SKIPEN pin can be used to select different operation modes. To enable the skip mode, SKIPEN must be set high. Skip mode is used to improve efficiency at light loads. In skip mode, the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with several pulses, and goes again into skip mode once the output voltage exceeds the set threshold voltage. The skip mode can be disabled by setting the SKIPEN to GND.

Power Save Mode

The SKIPEN pin can be used to select different operation modes. To enable power save, SKIPEN must be set high. Power save mode is used to improve efficiency at light load. In power save mode the converter only operates when the output voltage trips below a set threshold voltage. It ramps up the output voltage with one or several pulses and goes again into power save mode once the output voltage exceeds the set threshold voltage. This power save mode can be disabled by setting the SKIPEN to GND.

Low Battery Detector Circuit—LBI/LBO

The low-battery detector circuit is typically used to supervise the battery voltage and to generate an error flag when the battery voltage drops below a user-set threshold voltage. The function is active only when the device is enabled. When the device is disabled, the LBO pin is high-impedance. The switching threshold is 500 mV at LBI. During normal operation, LBO stays at high impedance when the voltage, applied at LBI, is above the threshold. It is active low when the voltage at LBI goes below 500 mV.

The battery voltage, at which the detection circuit switches, can be programmed with a resistive divider connected to the LBI pin. The resistive divider scales down the battery voltage to a voltage level of 500 mV, which is then compared to the LBI threshold voltage. The LBI pin has a built-in hysteresis of 10 mV. See the application section for more details about the programming of the LBI threshold. If the low-battery detection circuit is not used, the LBI pin should be connected to GND (or to VBAT) and the LBO pin can be left unconnected. Do not let the LBI pin float.

Low-EMI Switch

The device integrates a circuit that removes the ringing that typically appears on the SW node when the converter enters discontinuous current mode. In this case, the current through the inductor ramps to zero and the rectifying PMOS switch is turned off to prevent a reverse current flowing from the output capacitors back to the battery. Due to the remaining energy that is stored in parasitic components of the semiconductor and the inductor, a ringing on the SW pin is induced. The integrated antiringing switch clamps this voltage to VBAT and therefore dampens ringing.

LDO

The built-in LDO can be used to generate a second output voltage derived from the dc/dc converter output, from the battery, or from another power source like an ac adapter or a USB power rail. The LDO is capable of being back biased. This allows the user to connect the outputs of dc/dc converter and LDO. So the device is able to supply the load via dc/dc converter when the energy comes from the battery and efficiency is most important and from another external power source via the LDO when lower efficiency is not critical. The LDO must be disabled if the LDOIN voltage drops below LDOOUT and current flow is blocked. The status of the dc/dc stage (enabled or disabled) does not matter.

THERMAL INFORMATION

Implementation of integrated circuits in low-profile and fine-pitch surface-mount packages typically requires special attention to power dissipation. Many system-dependent issues such as thermal coupling, airflow, added heat sinks and convection surfaces, and the presence of other heat-generating components affect the power-dissipation limits of a given component.

Three basic approaches for enhancing thermal performance are listed below.

- Improving the power dissipation capability of the PCB design.
- Improving the thermal coupling of the component to the PCB.
- Introducing airflow in the system.

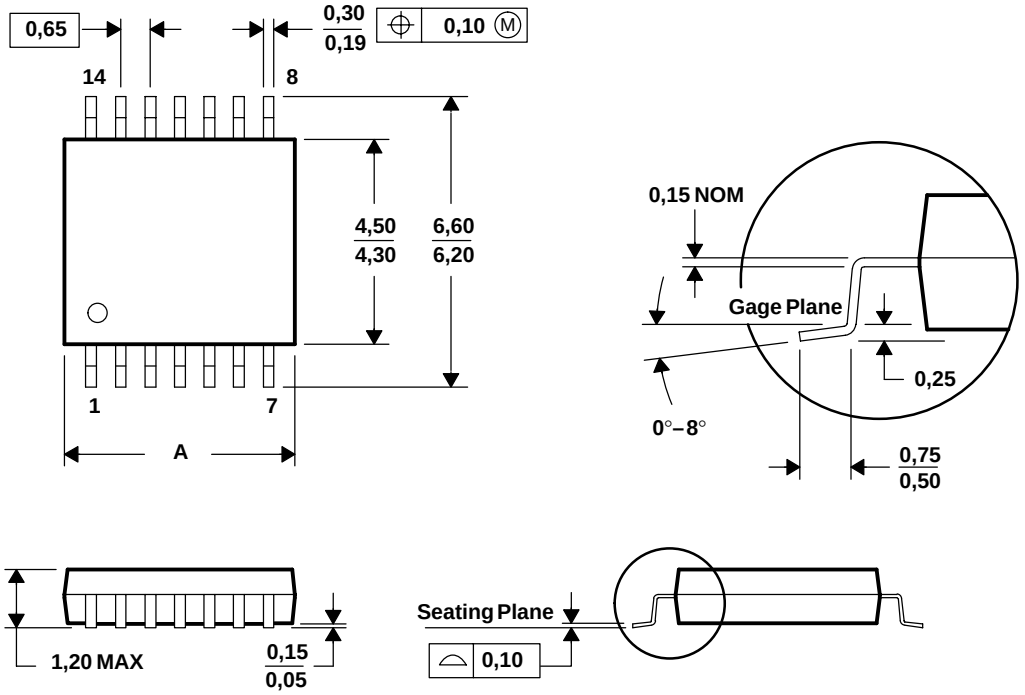
The maximum junction temperature (T_J) of the TPS6113x devices is 150°C. The thermal resistance of the 20-pin TSSOP package (PW) is $R_{\theta JA}$ = 155 K/W. Specified regulator operation is assured to a maximum ambient temperature T_A of 85°C. Therefore, the maximum power dissipation is about 420 mW. More power can be dissipated if the maximum ambient temperature of the application is lower.

$$P_{D(MAX)} = \frac{T_{J(MAX)} - T_A}{R_{\theta JA}} = \frac{150°C - 85°C}{155\ k/W} = 420\ mW \quad (9)$$

MECHANICAL DATA

PW (R-PDSO-G)** **PLASTIC SMALL-OUTLINE PACKAGE**

14 PINS SHOWN



DIM \ PINS **	8	14	16	20	24	28
A MAX	3,10	5,10	5,10	6,60	7,90	9,80
A MIN	2,90	4,90	4,90	6,40	7,70	9,60

4040064/F01/97

NOTES:A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-153

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